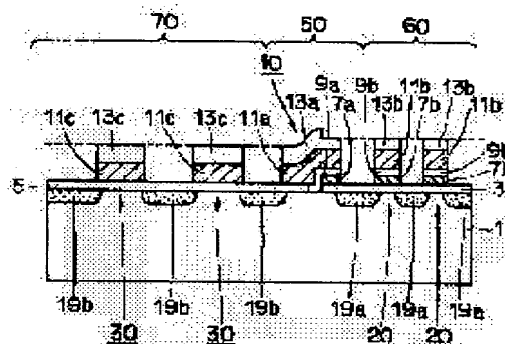


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(22) Date of filing : 18.11.1994 (72) Inventor : KUNORI YUUCHI

CONSTITUTION: There are a memory transistor region 60, a selective transistor region 70, and a separating region 50 for separating these two regions, within a memory cell array. In the memory cell region 60 is a stack gate type of memory transistor 20 made. In the selective transistor region 70 is a selective transistor region 30 made. In the separating region 50 is a first conductive layer 7a made through an gate insulating layer 3 on a silicon substrate 1. On the upper surface and the side of the first conductive layer 7a is an interlayer insulating layer 9a made. Moreover, on the silicon substrate 1 are second conductive layer 11a and an insulating layer 13a stacked through a gate insulating layer 5 and besides so that they may ride on the first conductive layer 7a.



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